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(71) Applicants: **INFINEON TECHNOLOGIES NORTH AMERICA CORP.** [US/US]; 1730 North First Street, San Jose, CA 95112-4508 (US). **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, NY 10504 (US).

(72) Inventors: **LU, Zhijian**; 510 Maloney Road, Poughkeepsie, NY 12603 (US). **MOREAU, Wayne**; 10 Lydia Drive, Wappingers Falls, NY 12590 (US). **CHEN, Kuang, Jung**; 19 Panessa Drive, Poughkeepsie, NY 12603 (US). **MACK, George**; P.O. Box 139, Pleasant Valley, NY 12569 (US).

(74) Agents: **BRADEN, Stanton, C.** et al.; Siemens Corporation, Intellectual Property Dept., 186 Wood Avenue South, Iselin, NJ 08830 (US).

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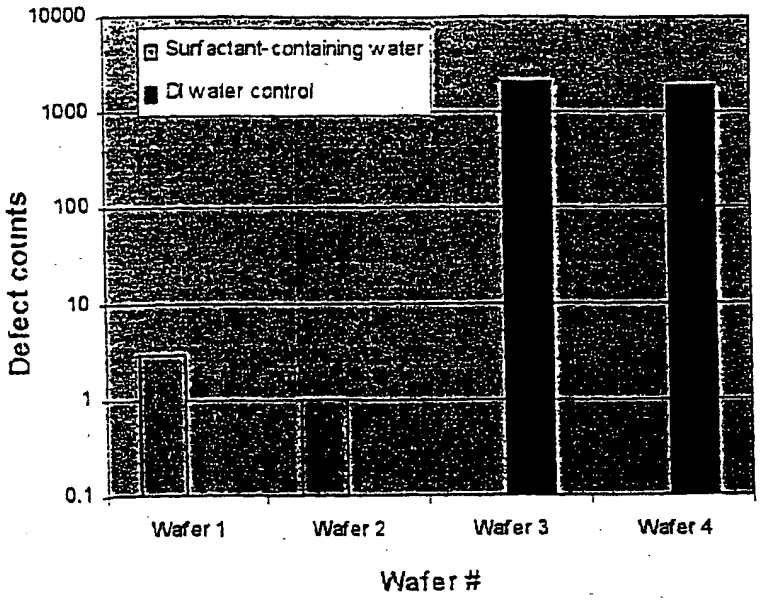
(54) Title: A METHOD TO REDUCE POST-DEVELOPMENT DEFECTS WITHOUT SACRIFICING THROUGHPUT



(57) Abstract: Post-development defects in the manufacture of semiconductor devices through the use of surfactants incorporated in the rinse water or the developer for the resist. The surfactants effectively remove resist defects in or around the resist pattern without attacking the resist itself.

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A METHOD TO REDUCE POST-DEVELOPMENT DEFECTS WITHOUT SACRIFICING THROUGHPUT

DESCRIPTION

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to the manufacture of semiconductor devices and, more particularly, to a method to reduce post-development defects in semiconductor devices without sacrificing throughput.

Background Description

As the minimum feature size of semiconductor devices becomes smaller and smaller, defect control becomes more and more important and challenging particularly for achieving a high product yield. Starting from the qualification of 256M DRAM (Dynamic Random Access Memory) technology, a class of special defects so called "Blob Defects" was discovered on a nested contact hole level of bit line contact CB when using chrome on glass and JSR M20G resist. Later on, it was found that blob defects exist in almost all DUV resist, such as Shipley UV2HS, UV6HS and JSR M60G, regardless of whether it is ESCAP resists or Acetal resists. Actually, the better the resist contrast and surface inhibition is, usually the higher the blob density is. Therefore, selection of contact hole resists for patterning even smaller contact hole size has to face a compromise between defect density and resist lithographic performance, which is not compatible with the trend of low k1 printing. Moreover, no resist evaluated so far shows zero blob density. Blob defects become a limiting factor in resist selection and yield enhancement.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to minimize or eliminate post-development defects.

It is another object of the invention to improve product yield by preventing missing patterns caused by defects.

It is also an object to minimize pattern collapse.

According to the invention, surfactants are incorporated into rinse water or the resist developer. The surfactants effectively remove resist defects in or around the resist pattern without attacking resist itself.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 is a scanning electron microscope (SEM) microphotograph showing a blob defect; and

Figure 2 is a graph showing the effect of surfactant-containing water on defect removal.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

Referring now to the drawings, and more particularly to Figure 1, there is shown the morphology of a typical blob defect. This type of defect potentially limits feature size of semiconductor devices and reduces product yield.

The invention incorporates suitable surfactants into rinse de-ionized

(DI) water for defect removal. The surfactant containing DI water would be applied to the resist after patterning and development of the resist. The concentration of surfactants can range from 0.001 to 10%. In a preferred embodiment, the surfactant used was ammonium lauryl sulfate in a concentration ranging from 0.01% to 1%. However, any surfactants with a similar hydrophilic-lipophilic balance (HLB) to ammonium lauryl sulfate will work in removing defects. The surfactant-containing water rinse can be conducted in either a dynamic way (streamline) or a static way (puddle rinse). The time of application can vary from a few seconds to hundreds of seconds. The temperature range can vary from 10°C to 100°C. The surfactants can also be incorporated directly into the developer for defect removal.

Figure 2 shows the effect of surfactant-containing water on defect removal. The resist used in these experiments were Shipley UV83 530nm plus Shipley ARC AR3 90nm. Wafers 1 and 2 were rinsed with surfactant containing de-ionized water, while wafers 3 and 4 were rinsed with de-ionized water without surfactants. Under the exactly same process conditions, the use of surfactant-containing rinse water leads to three orders of magnitude of defect reduction compared to that of pure DI water rinse.

While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A method to reduce post-development defects in the manufacture of semiconductor devices comprising the steps of:

incorporating suitable surfactants into one of de-ionized rinse water and resist developer; and

applying the surfactant containing de-ionized rinse water or resist developer to a patterned resist on a semiconductor substrate.

2. A method as in claim 1, wherein said surfactants have a concentration ranging from 0.001 to 10%.

3. A method as in claim 1, wherein the surfactant is ammonium lauryl sulfate.

4. A method as in claim 3, wherein the ammonium lauryl sulfate has a concentration ranging from 0.01 to 1%.

5. A method as in claim 1, wherein said surfactants are incorporated directly into said resist developer.

6. A method as in claim 1, wherein said surfactants are incorporated into said de-ionized rinse water used in a dynamic rinse process.

7. A method as in claim 1, wherein said surfactants are incorporated into said de-ionized rinse water used in a static rinse process.

8. A method as in claim 1, wherein said surfactants are incorporated into said

de-ionized rinse water used in a rinse process lasting between 1 and 1000 seconds.

9. A method as in claim 6, wherein the temperature of said surfactants containing rinse water ranges from 10°-100°C.

10. A method as in claim 9, wherein the surfactant is ammonium lauryl sulfate.

11. A method as in claim 10, wherein the ammonium lauryl sulfate has a concentration ranging from 0.01 to 1%.

12. A resist developer used or developing resists used in semiconductor manufacture, said resist developer containing a surfactant.

13. The resist developer as in claim 12, wherein the surfactant is ammonium lauryl sulfate.

14. The resist developer as in claim 13, wherein the ammonium lauryl sulfate has a concentration ranging from 0.01 to 1%.

15. A rinse for rinsing developed resists used in semiconductor manufacturer comprising de-ionized water and a surfactant.

16. The rinse as in claim 15, wherein the surfactant is ammonium lauryl sulfate.

17. The rinse as in claim 16, wherein the ammonium lauryl sulfate has a concentration ranging from 0.01 to 1%.

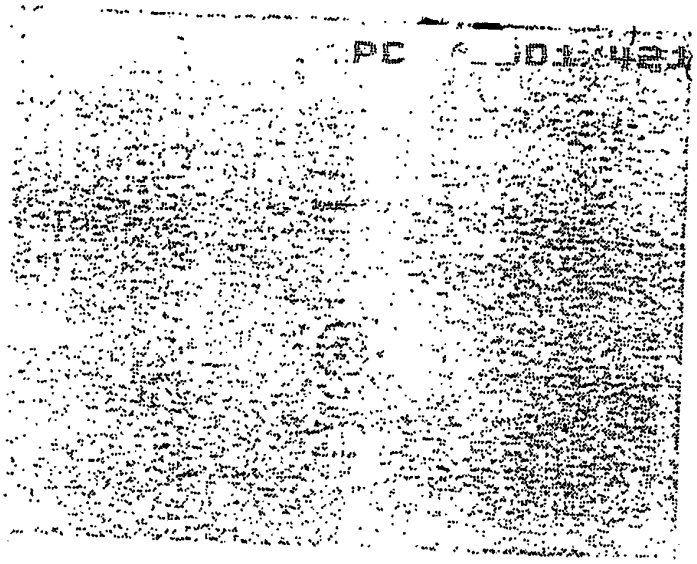

FIG. 1

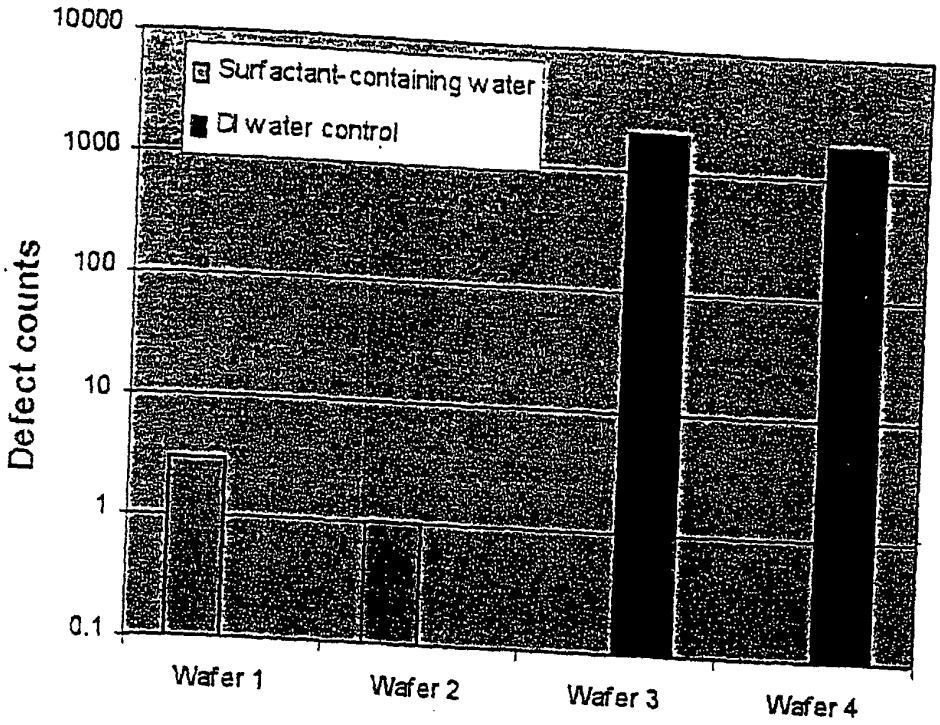
10000
1000
100
10
1
0.1
Defect counts
Surfactant-containing water
DI water control
Wafer 1
Wafer 2
Wafer 3
Wafer 4
Wafer #

FIG. 2

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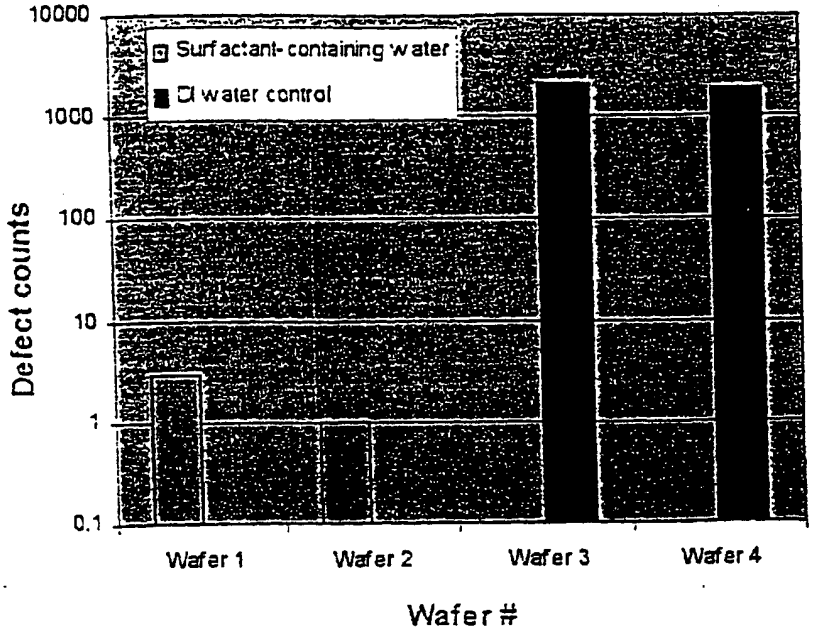

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INT' 'NATIONAL SEARCH REPORT

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B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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EPO-Internal, CHEM ABS Data

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[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

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